26. (New) The semiconductor device according to claim 21, wherein the semiconductor substrate is an SOI substrate.

27. (New) The semiconductor device according to claim 21, further comprising:

an element isolating region formed within the semiconductor substrate such that the second gate insulating film and the second conductive film extend over said element isolating region;

a contact electrically connected to a portion of the second conductive film which is positioned on the element isolating region; and

a wiring electrically connected to said contact.

28. (New) The semiconductor device according to claim 21, wherein a plurality of second concave portions are formed in the semiconductor substrate such that the second concave portions are filled with the second gate insulating film and the second conductive film, and a surface of the second conductive film is substantially flat.

29. (New) The semiconductor device according to claim 28, wherein a plurality of gate electrodes each consisting of the second conductive film is formed in said second concave portions.

30. (New) The semiconductor device according to claim 21, wherein an impurity concentration in the second conductive film is higher than an impurity concentration in the semiconductor substrate.

31. (New) The semiconductor device according to claim 21, wherein said second insulating film functions as an insulating film for an anti-fuse portion or for a capacitor element.

REMARKS

The office action of September 6, 2002 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-11 remain pending. New claims 21-31 have been added. Claims 12-20 have been canceled without prejudice or disclaimer. Applicants reserve the right to pursue the subject

matter of the non-elected claims in a divisional application prior to termination of the instant proceedings.

Applicants have removed the incorporation by reference to the priority document as no essential material is contained in said document.

Applicants have amended the specification to correct various minor informalities discovered therein and to otherwise better clarify the invention.

Claims 1-11 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants have amended the claims to correct various antecedence informalities and to otherwise clarify the invention. Applicants submit that the claims are sufficiently definite to comply with section 112.

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of U.S. patent no. 5,629,227 to Chen, U.S. patent no. 6,130,469 to Bracchitta et al. ("Bracchitta"), and Wolf, S., "Silicon Processing of the VLSI Era,", Vol. 2 Process Integration ("Wolf"). Applicants respectfully traverse this rejection.

Amended claim 1 recites, among other features, a first concave portion for element isolation, formed in a semiconductor substrate, a second concave portion formed in the semiconductor substrate and having a depth from a top surface of the semiconductor substrate, equal to a depth of the first concave portion.

Neither Chen, Bracchitta nor Wolf alone or in combination teaches or suggests a first and second concave portion as called for in claim 1. Notably, in Bracchitta, the STI portion 32 does not have a depth from a top surface of the semiconductor substrate, equal to a depth of the portion for antifuse formed in the recessed gate 40. Neither Chen nor Wolf remedy this defect and thus the combination of Chen, Bracchitta, even if proper, does not result in a second concave portion formed in the semiconductor substrate and having a depth from a top surface of the semiconductor substrate, equal to a depth of the first concave portion as recited in claim 1. Thus, claim 1 is patentably distinct from the applied combination. Claims 2-11, which directly or indirectly depend from claim 1, are patentable over the applied art for the same reasons as claim 1, and further in view of the additional novel features recited therein.

New claims 21-31 are fully supported by the specification and considered allowable over the art of record. For example, claim 21 calls for, a first concave portion formed in a semiconductor substrate for serving as an aligning mark portion. None of the art of record alone or in combination teaches or suggests the claim 21 combination of features including such a feature.

CONCLUSION

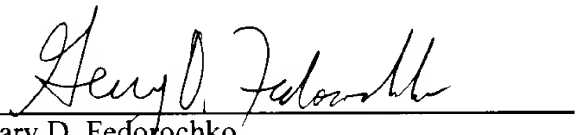
It is believed that no fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

All rejections having been addressed, applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: December 6, 2002

By: 

Gary D. Fedorochko
Registration No. 35,509

1001 G Street, N.W.
Washington, D.C. 20001-4597
(202) 508-9100

GDF:lab

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph starting on page 1, line 5, has been amended as follows:

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2000-039968, filed February 17, 2000~~, the entire contents of which are incorporated herein by reference~~.

The paragraph starting on page 5, line 9, has been amended as follows:

The anti-fuse is expected to produce various merits. For example, the anti-fuse is expected to decrease the ~~occupies~~ area occupied within the chip and to permit replacing the final defective cell after sealing the package ~~sealing~~. Also, in the anti-fuse, a desired gate insulating film is broken to make the device conductive by applying a voltage higher than the breakdown voltage. Therefore, in general, the anti-fuse is connected to a high voltage generating circuit for breaking the gate insulating film and to a judging circuit for detecting whether the anti-fuse portion is broken or not. It follows that, in breaking the anti-fuse portion, the gate insulating film in the judging circuit portion also is~~receives a~~ damaged to some extent. Such being the situation, it was desirable to permit the anti-fuse portion to be broken with a reasonably low voltage while suppressing the damage done to the judging circuit and other portions as much as possible.

The paragraph starting on page 9, line 20, has been amended as follows:

It is possible to form the second gate electrode on the bottom surface of the third concave portion, on ~~the~~ both side surfaces or one side surface of the third concave portion, and on the semiconductor substrate.

The paragraph starting on page 14, line 17, has been amended as follows:

FIG. 22A is ~~an~~ a plan view showing the case where a gate electrode for a plurality of anti-fuses is formed in a single concave portion;

VERSION WITH MARKINGS TO SHOW CHANGES MADE

The paragraph starting on page 14, line 22, has been amended as follows:

FIG. 23A is ~~an~~a plan view showing the case where a concave portion is filled with a gate electrode for an anti-fuse and a contact is formed on an element isolating region;

The paragraph starting on page 19, line 16, has been amended as follows:

According to the first embodiment of the present invention described above, the gate insulating film 18 for the anti-fuse is formed on a bottom surface of the third concave portion 14. It should be noted that ~~a damage~~damage is done to the bottom surface of the third concave portion 14 by the RIE process employed for forming the concave portions 12, 13 and 14. Therefore, it is possible to lower the breakdown voltage of the gate insulating film 18b formed in the concave portion 14, compared with the gate insulating film 18a of the transistor formed on the surface of the substrate 11. It follows that it is possible to break only the gate insulating film 18b for the anti-fuse without applying an extremely high voltage. This makes it possible to suppress the damage done to the gate insulating film 18a of the transistor included in, for example, a judging circuit portion. It follows that it is possible to maintain a high reliability of the transistor and to improve the yield.

The paragraph starting on page 21, line 2, has been amended as follows:

For example, where the lower end portion of the resist film 17 is positioned inside the upper edge portion of the third concave portion 14, it is possible to permit the silicon oxide film 15 to remain partly within the third concave portion 14, as shown in FIG. 7. It should be noted that, in the step of forming the gate electrode, ~~a~~ damage is done to the gate insulating film in the edge portion of the gate electrode in the step of, for example, the RIE process, making it impossible to adjust completely the nonuniformity in the breakdown voltage of the gate electrode. However, in the structure shown in FIG. 7, the remaining silicon oxide film 15 resides in the edge portion of the gate electrode 24. It follows that the breakdown at the edge portion of the gate electrode 24 can be suppressed by the insulating film formed of the silicon oxide film

VERSION WITH MARKINGS TO SHOW CHANGES MADE

15, making it possible to adjust the nonuniformity in the breakdown voltage of the gate insulating film 18b.

The paragraph starting on page 22, line 16, has been amended as follows:

According to the second embodiment, the corner portions 14a and 14b of the concave portion 14 are used as the anti-fuse. Therefore, the electric field concentration occurs on particularly the corner portions 14a and 14b so as to make it possible to break effectively the gate insulating film 18b.

The paragraph starting on page 24, line 8, has been amended as follows:

It should be noted that the polysilicon film 19 and the silicon nitride film 21 are formed in many cases by, for example, an LPCVD (Low Pressure Chemical Vapor Deposition) method that is carried out under high temperatures, e.g., several hundred ℃. Therefore, stress derived from the difference in the thermal expansion coefficient is generated under room temperature under which the semiconductor device is actually used. It follows that the breakdown voltage of the anti-fuse portion can be further lowered, compared with the semiconductor device shown in, for example, FIGS. 8 and 9. It should also be noted that, since the gate electrode 24 extends onto the silicon substrate 11, the gate electrodes 22 and 24 for the transistor and the anti-fuse ~~can~~could be formed in the same height in the lithography step for forming the gate electrodes 22 and 24. This facilitates the lithography step and further improves the yield. Incidentally, the structure shown in FIG. 12 produces the effect that a position alignment between the contact plug 28 and the tungsten film 20 is easy, compared with the structure shown in FIG. 11.

The paragraph starting on page 25, line 12, has been amended as follows:

In each of the first and second embodiments of the present invention described above, the silicon oxide film 15 within the concave portion 14 is removed completely in the stepping process shown in FIG. 3. However, it is not absolutely necessary in the present invention to remove completely the silicon oxide film 15 within the concave portion 14. For example, it is

VERSION WITH MARKINGS TO SHOW CHANGES MADE

also possible to leave the silicon oxide film 15 unremoved in a part of the concave portion 14, as shown in FIG. 14. In this case, even if ~~a~~ damage is done to the bottom surface of the concave portion 14 in the RIE step for forming the concave portion 14, it is possible to suppress the nonuniformity in the breakdown voltage of the gate insulating film by forming the silicon oxide film 15 on the bottom surface of the concave portion 14 after formation of the concave portion 14.

The paragraph starting on page 26, line 10, has been amended as follows:

Also, as shown in FIG. 15, it is possible to form the contact plug 28 for the electrical connection to the gate electrode (not shown) of another element above the element isolating region 16. Where a contact hole is formed on an element region, ~~a damage~~damage is done to the gate insulating film right under the contact hole in the RIE step for forming the contact hole, giving rise to a possibility of generating a nonuniformity in the breakdown voltage. In the case of the structure shown in FIG. 15, however, it is possible to suppress the nonuniformity in the breakdown voltage derived from the damage generated in the step of forming the contact hole because the contact hole is formed above the element isolating region.

The paragraph starting on page 27, line 26, has been amended as follows:

As shown in FIG. 18, the conductivity type, e.g., P-type, of a well 32a formed in a surface region of the silicon substrate 11 is made equal to that of a polysilicon film 19a. As a result, it is possible to lower the resistance of the anti-fuse portion after breakdown of the gate insulating film 18b so as to improve the accuracy of ~~judgement~~judgment of breakdown/non-breakdown.

The paragraph starting on page 28, line 22, has been amended as follows:

Also, as shown in FIG. 20, the conductivity, e.g., N-type, of the well 32b formed in a surface region of the silicon substrate 11 is made equal to that of the polysilicon film 19b, and the impurity concentration in the polysilicon film 19b is made higher by at least one place than

VERSION WITH MARKINGS TO SHOW CHANGES MADE

that in the well 32b. Incidentally, in this apparatus, a positive electric field is imparted to the gate electrode 24 in breaking down the gate insulating film 18b in the anti-fuse portion, and a negative electric field is imparted to the gate electrode 24 when the apparatus is actually used for performing the ~~judgement~~judgment. Where the polarities of the electric field in the breakdown step and the judging step are made opposite to each other, the depletion layer formed in the well 32b on the lower side of the gate is thickened in the judging step because the impurity concentration in the well 32b is lower than that in the polysilicon film 19b. As a result, only an effectively low electric field is applied to the gate insulating film in the anti-fuse portion that was not broken down. It follows that it is possible to increase the reliability of the judging operation that is repeatedly performed in actually using the apparatus.

The paragraph starting on page 31, line 2, has been amended as follows:

Also, the damaged layer in the uppermost surface of the silicon substrate 11 can be removed by etching thin the surface of the silicon substrate 11 by an isotropic etching such as a CDE (Chemical Dry Etching) method in removing the silicon oxide film 15 in the stepping process shown in FIG. 3. It is also possible to weaken the effect of the electric field concentration by rounding~~making roundish~~ the corner portions 14a and 14b of the concave portion 14. The breakdown voltage rendered lower than a predetermined value can be restored to some extent by these methods, too.

The paragraph starting on page 31, line 13, has been amended as follows:

By ~~contraries~~contrast, where it is desired to further lower the breakdown voltage, it is possible to further introduce damages to the bottom surface of the concave potion 14 by using a RIE method having a high power in place of the wet etching method in removing the silicon oxide film 15 in the stepping process.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

The paragraph starting on page 31, line 19, has been amended as follows:

Further, after removal of the silicon oxide film 15 in the stepping process, an impurity ion is introduced by using the ion implantation technology before the resist film 17 is peeled off. As a result, it is possible to control the thickness of the gate oxide film 18 formed in the subsequent process. It follows that it is possible to control the breakdown voltage of the gate insulating film 18b. For example, after the lithography process for the stepping, ~~ana~~ a nitrogen ion implantation is performed. Thereby it is possible to form the thin thickness of the gate oxide film 18 formed in the subsequent process, it is possible to gain the breakdown voltage of the predetermined value by the film 18 beingis used as anti-fuse. In this case, the stepped portion of the anti-fuse portion is not always a necessity, however it is possible to lower the breakdown voltage by the stepped portion.

The paragraph starting on page 33, line 26, has been amended as follows:

In general, a capacitor element is formed in many cases within the semiconductor device for stabilizing the power source. In this embodiment, used is a capacitor formed of a gate insulating film 48, as shown in FIG. 26. For further stabilizing the power source, it is necessary to form a capacitor having a larger capacitance within the semiconductor device. However, in recent years, the area occupied by the capacitor for stabilizing the power source has beenis rendered large relative to the area of the entire chip so as to increase the manufacturing cost of the semiconductor device. Such being the situation, it is required to diminish the area occupied by the capacitor for stabilizing the power source.

The paragraph starting on page 35, line 13, has been amended as follows:

According to the fifth embodiment, the concave portion 14 of the silicon substrate 11 can be used as a capacitor element for stabilizing the power source, not as the anti-fuse element, because a silicon oxynitride film whose breakdown voltage is unlikely to be lowered is used as the gate insulating film 18b'. Also, the surface area of the gate insulating film 18b' can be increased by forming a plurality of concave portions 14 within the silicon substrate 11. It

VERSION WITH MARKINGS TO SHOW CHANGES MADE

follows that the capacitance of the capacitor can be increased without increasing the area occupied by the capacitor.

IN THE CLAIMS:

1. (Amended) A semiconductor device, comprising:

a first concave portion for element isolation, formed in a semiconductor substrate;

a second concave portion formed in the semiconductor substrate and having a depth from a top surface of the semiconductor substrate, equal to a depth of the first concave portion;

a first gate insulating film formed ~~selectively~~ on a selected portion of said semiconductor substrate;

a second gate insulating film formed in at least ~~the~~ a bottom surface of said second concave portion;

a first conductive film formed on said first gate insulating film; and

a second conductive film formed on said second gate insulating film.

2. (Amended) The semiconductor device according to claim 1, wherein the second gate insulating film and the second conductive film are formed on the bottom surface of the second concave portion, on at least one side surface of the second concave portion and on the semiconductor substrate, and ~~the~~ a top surface of the first conductive film is flush with ~~the~~ a surface of the second conductive film formed on the semiconductor substrate.

3. (Amended) The semiconductor device according to claim 1, wherein the second gate insulating film is formed in ~~the~~ a corner portion of the second concave portion.

4. (Amended) The semiconductor device according to claim 1, wherein an insulating film is formed on the second conductive film, and the second concave portion is filled with the insulating film, the second gate insulating film and the second conductive film.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

5. (Amended) The semiconductor device according to claim 1, wherein the second concave portion is filled with the second gate insulating film and the second conductive film, and ~~the~~ a surface of the second conductive film is substantially flat.

7. (Amended) The semiconductor device according to claim 1, further comprising:

an element isolating region formed within the first concave portion ~~semiconductor substrate~~ such that the second gate insulating film and the second conductive film are allowed to extend over said element isolating region;

a contact electrically connected to ~~that~~ a portion of the second conductive film which is positioned on the element isolating region; and

a wiring electrically connected to said contact.

8. (Amended) The semiconductor device according to claim 1, wherein a plurality of second concave portions are formed in the semiconductor substrate such that ~~these~~ the second concave portions are filled with the second gate insulating film and the second conductive film, and ~~the~~ a surface of the second conductive film is substantially flat.

9. (Amended) The semiconductor device according to claim 1, wherein a plurality of gate electrodes each consisting of the second conductive film is formed in said second concave portions.

10. (Amended) The semiconductor device according to claim 1, wherein ~~the~~ an impurity concentration in the second conductive film is higher than ~~that~~ an impurity concentration in the semiconductor substrate.

11. (Amended) The semiconductor device according to claim 1, wherein said second insulating film functions as ~~the~~ an insulating film for ~~the~~ an anti-fuse portion or for ~~the~~ a capacitor element.